Amendments to the Claims:

Please amend claims 1 and 2 as follows.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Currently Amended) A semiconductor substrate having a multi-layered spacer, comprising:

a plurality of gate electrodes each including a gate oxide layer, a gate conductive layer, and a capping dielectric layer formed on [[a]] the semiconductor substrate;

a gate polyoxide layer formed on sidewalls of the gate oxide layer and the gate conductive layer and being in contact with a ~~predetermined~~ portion of the semiconductor substrate;

a silicon nitride layer being in contact with [[the]] sidewalls of the capping dielectric layer and in contact with the gate polyoxide layer;

an oxide layer being in contact with an outer surface of the silicon nitride layer; [[and]]

an anisotropically etched external spacer being in contact with an outer surface of the oxide layer;

a portion of the semiconductor substrate exposed between neighboring gate electrodes by etching the oxide layer, silicon nitride layer and gate polyoxide layer using the external spacers and the gate electrodes as an etch mask so that outer ends of the gate polyoxide layer, the silicon nitride layer, and the oxide layer, and a lower outer end of the external spacer are aligned; and

a conductive pad in a region between adjacent gate electrodes having the multi-layered spacer and being in contact with the exposed semiconductor substrate and the external spacer.

2. (Currently Amended) The semiconductor substrate of claim 1, further comprising:

~~a pad formed in a region between adjacent gate electrodes having the multi-layered spacer and being in contact with the semiconductor substrate; and~~

an interlevel dielectric layer formed on the pad and each gate electrode having the multi-

layered spacer.

3. (Original) The semiconductor substrate of claim 1, wherein the gate polyoxide layer prevents the silicon nitride layer from separating from the semiconductor substrate and has a thickness of about 50 ~ 100 Å.

4. (Original) The semiconductor substrate of claim 1, wherein the gate polyoxide layer is an oxide layer formed at a temperature of about 800 ~ 900 °C with the injection of oxygen.

5. (Original) The semiconductor substrate of claim 1, wherein the silicon nitride layer has a thickness of about 100 ~ 500 Å.

6. (Original) The semiconductor substrate of claim 1, wherein the oxide layer is an oxide layer formed at a temperature of about 600 ~ 800 °C using $SiCl_4$ and O_2.

7. (Original) The semiconductor substrate of claim 1, wherein the oxide layer is a middle temperature oxide layer or a high temperature oxide layer having a dielectric constant of 3.9, and has a thickness of about 100 ~ 500 Å.

8. (Original) The semiconductor substrate of claim 1, wherein the external spacer is formed of silicon nitride or silicon oxynitride.